IN THE CLAIMS:

1. (Currently Amended) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles; [[and]]

treating the silicon tile edges to minimize the generation of contaminating particles; and

following the treating of the silicon tile edges, chemically etching the silicon tile surfaces.

2. (Original) The method of claim 1 wherein shaping silicon tiles includes cutting tiles from a silicon ingot using a method selected from the group including saw cutting, laser cutting, high pressure water cutting, and router cutting.

3. (Original) The method of claim 1 wherein shaping the silicon tiles includes cutting the silicon tiles to a thickness in the range of 7 millimeters (mm) to 10 mm.

4. (Original) The method of claim 1 wherein treating the silicon tiles includes subjecting the silicon tile top and bottom surface edges to a treatment selected from the group including beveling and radiusing.

5. (Original) The method of claim 4 wherein the silicon tile top surface edges are beveled within the range of 1 mm to 5 mm.

6. (Original) The method of claim 4 wherein the silicon tile top surface edges are radiused within the range of 3 mm to 10 mm.

7. (Original) The method of claim 4 wherein the silicon tile bottom surface edges are beveled approximately 1.5 mm.

8. (Original) The method of claim 1 wherein treating the silicon tiles includes subjecting the silicon tile corners to a treatment selected from the group including beveling and radiusing.

9. (Original) The method of claim 8 wherein the silicon tile corners are beveled approximately 1.5 mm.

10. (Original) The method of claim 1 wherein shaping silicon tiles includes shaping silicon tiles from a material selected from the group including single-crystal silicon (c-Si) and polycrystalline silicon (p-Si).

11. (Original) The method of claim 1 wherein shaping silicon tiles includes shaping silicon tiles from a silicon material doped with a p-type dopant with a resistivity in the range from 0.5 to 50 ohms per centimeter.

12. Canceled

13. (Currently Amended) The method of claim [[12]] 1 wherein chemically etching the silicon tile surfaces includes removing silicon material within the range of 50 microns (um) to 500 um.

14. (Currently Amended) The method of claim [[12]] 1 wherein chemically etching the silicon tile surfaces includes immersing the silicon tiles in a solution selected from the group including HNO3~~HMO3~~/HF/CH3COOH (4:1:3) and HF/HNO3 (1.6:1.8).

15. (Currently Amended) The method of claim [[12]] 1 wherein chemically etching the silicon tile surfaces includes immersing the silicon tiles in a solution that is a mixture of HNO3 and HF, with traces of CH3COOH.

16. (Currently Amended) The method of claim [[12]] 1 further comprising:

following the chemically etching of the silicon tiles, polishing the silicon tile top and bottom surfaces to a predetermined flatness.

17. (Original) The method of claim 16 wherein polishing the silicon tile top and bottom surfaces includes polishing the surfaces with a process selected from the group including sanding with small grit paper and chemical-mechanical polishing (CMP) with a SiO2 slurry.

18. (Original) The method of claim 16 wherein polishing the silicon tile top and bottom surfaces includes polishing the surfaces to a flatness in the range of 5 um to 10 um.

19. (Original) The method of claim 16 wherein polishing the silicon tile top and bottom surfaces includes polishing the surfaces to a flatness in the range of 1 um to 6 um.

20. (Original) The method of claim 16 wherein polishing the silicon tile top and bottom surfaces includes polishing the surfaces to a flatness in the range of 0.1 um to 1 um.

21. (Original) The method of claim 16 further comprising:

following the polishing of the silicon tiles, attaching a plurality of the silicon tiles to a backing plate to form a completed silicon target.

22. (Original) The method of claim 21 wherein attaching a plurality of the silicon tiles to a backing plate to form a completed silicon target includes forming a silicon target with a surface of approximately 650 mm by 550 mm.

23. (Original) The method of claim 22 wherein shaping silicon tiles includes shaping the tiles from a polycrystalline silicon material; and

wherein attaching a plurality of silicon tiles to a backing plate includes attaching four polycrystalline silicon tiles.

24. (Original) The method of claim 22 wherein shaping silicon tiles includes shaping the tiles from a single-crystal silicon material; and

wherein attaching a plurality of silicon tiles to a backing plate includes attaching twenty single-crystal silicon tiles.

25. (Original) The method of claim 21 wherein attaching a plurality of silicon tiles to a backing plate includes attaching each silicon tile with adhesive placed on the silicon tile bottom surface, along the bottom surface edges to form an adhesive boundary, with indium placed inside the adhesive boundary.

26. (Original) The method of claim 1 wherein shaping silicon tiles includes shaping the silicon tiles having a (100) orientation.

27. (Original) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for a forming a silicon (Si) target, the method comprising:

cutting silicon tiles to a thickness in the range from 7 millimeters (mm) to 10 mm;

subjecting the silicon tile top and bottom surface edges to a treatment selected from the group including beveling and radiusing;

beveling the silicon tile corners approximately 1.5 mm;

chemically etching the silicon tile surfaces to remove silicon material within the range of 50 microns (um) to 500 um;

polishing the silicon tile top and bottom surfaces to a predetermined flatness within the range of 0.1 um to 10 um; and,

attaching a plurality of the silicon tiles to a backing plate to form a completed silicon target.

28. (Original) The method of claim 27 wherein subjecting the silicon tile top surface edges to a treatment includes beveling the top surfaces edges within the range of 1 mm to 5 mm.

29. (Original) The method of claim 27 wherein subjecting the silicon tile top surface edges to a treatment includes radiusing the top surface edges within the range of 3 mm to 10 mm.

30. (Original) The method of claim 27 wherein subjecting the silicon tile bottom surface edges to a treatment includes beveling the bottom surface edges approximately 1.5 mm.

31. (Original) The method of claim 27 wherein chemically etching the silicon tile surfaces includes immersing the silicon tiles in a solution that is a mixture of HNO3 and HF, with traces of CH3COOH.

32. (Original) The method of claim 27 wherein attaching a plurality of the silicon tiles to a backing plate to form a

completed silicon target includes forming a silicon target with a surface of approximately 650 mm by 550 mm.

33-61. Canceled

62. (New) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles;

treating the silicon tile edges, to minimize the generation of contaminating particles, by:

subjecting the silicon tile bottom surface edges to a treatment selected from the group including beveling and radiusing; and

beveling the silicon tile top surface edges within the range of 1 mm to 5 mm.

63. (New) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles;

treating the silicon tile edges, to minimize the generation of contaminating particles, by:

subjecting the silicon tile bottom surface edges to a treatment selected from the group including beveling and radiusing; and

radiusing the silicon tile top surface edges within the range of 3 mm to 10 mm.

64. (New) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles;

treating the silicon tile edges, to minimize the generation of contaminating particles, by:

subjecting the silicon tile top surface edges to a treatment selected from the group including beveling and radiusing; and

beveling the silicon tile bottom surface edges approximately 1.5 mm.

65. (New) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles; and

treating the silicon tile edges, to minimize the generation of contaminating particles, by beveling the silicon tile corners approximately 1.5 mm.

66. (New) In the fabrication of integrated circuit (IC) sputter deposited silicon films, a method for forming silicon (Si) target tiles, the method comprising:

shaping silicon tiles from a silicon material doped with a p-type dopant and a resistivity in the range from 0.5 to 50 ohms per centimeter; and

treating the silicon tile edges to minimize the generation of contaminating particles.